FEATURES

- Multi Mode PSR Control
- Quasi Resonant Operation for High Efficiency
- Audio Noise Free Operation
- Fast Dynamic Response
- Low Standby Power <70mW
- ±4% CC and CV Regulation
- Programmable Cable Drop Compensation (CDC) in PSR CV Mode
- Built-in AC Line & Load CC Compensation
- Build in Protections:
  - Short Load Protection (SLP)
  - On-Chip Thermal Shutdown (OTP)
  - Cycle-by-Cycle Current Limiting
  - Leading Edge Blanking (LEB)
  - Pin Floating Protection
  - VDD OVP & UVLO & Clamp
- Available with DIP7 Package

APPLICATIONS

- Battery Chargers for Cellular Phones
- AC/DC Power Adapter and LED Lightings

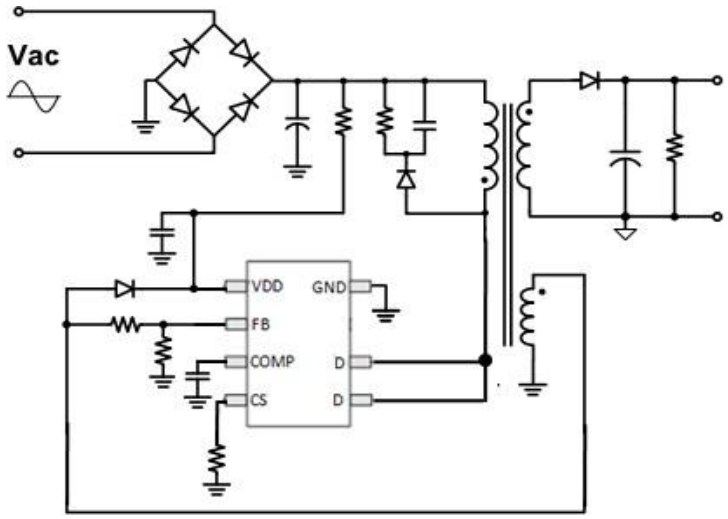
GENERAL DESCRIPTION

DP5546 is a high performance Quasi Resonant Primary Side Regulation (PSR) controller with high precision CV/CC control ideal for charger applications.

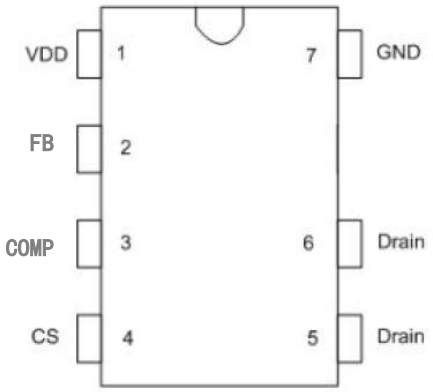
In CV mode, DP5546 adopts Multi Mode Control which uses the hybrid of AM (Amplitude Modulation) mode and (Frequency Modulation) FM mode to improve system efficiency and reliability. In CC mode, the IC uses QR control with CC loop regulation. The IC can achieve audio noise free operation and optimized dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

DP5546 integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), Gate Clamping, and VDD Clamping.

TYPICAL APPLICATION CIRCUIT



Pin Configuration



Marking Information

DP5546 for product name;

XXXXXX The first X represents the last year,2019 is 9;The second X represents the month,in A-L 12 letters;The third and fourth X on behalf of the date,01-31 said;The last two X represents the wafer batch code.

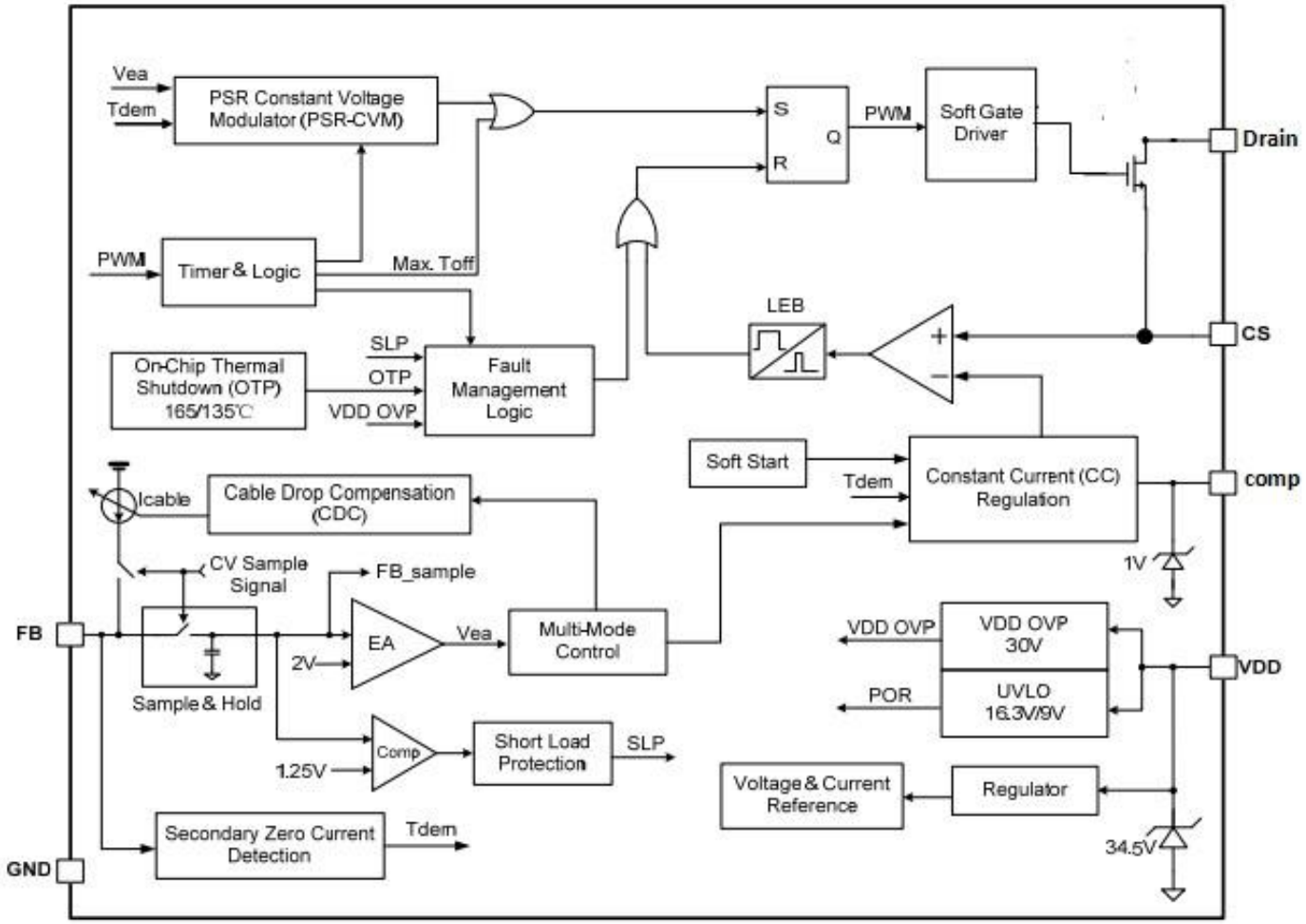
Pin Description

Pin Number	Pin Name	I/O	Description
1	VDD	P	Power Supply Pin of the Chip
2	FB	I	System feedback pin which regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding
3	COMP	I	Connect a capacitor between this pin and GND for CC regulation.
4	CS	I	Current Sense Input Pin
5/6	Drain	O	The Power MOSFET Drain.
7	GND	P	The Ground of the IC

Ordering Information

Part Number	Description
DP5546	DIP7, Rohs, 50Pcs/Tube

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	34.5	V
VDD DC Clamp Current	10	mA
Drain Voltage (off state)	-0.3 to 650	V
CS, CC voltage range	-0.3 to 7	V
FB voltage range	-0.7 to 7	V
Package Thermal Resistance----Junction to Ambient (SOP-7L)	250	^{o}C/W
Maximum Junction Temperature	175	^{o}C
Storage Temperature Range	-65 to 150	^{o}C
Lead Temperature (Soldering, 10sec.)	260	^{o}C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 27	V
Operating Ambient Temperature	-40 to 85	^{o}C
Maximum Switching Frequency	120	kHz

Electrical Characteristics (T_A= 25℃, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin			2	20	uA
I_{VDD_Op}	Operation Current	V_{FB}=3V,GATE=0.5nF, VDD=20V		1	1.5	mA
$I_{VDD\_standby}$	Standby Current			0.5	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		15	16.3	17.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		8	9	10	V
V_{DD_OVP}	VDD OVP Threshold		28	30	32	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	I(V_{DD}) = 7mA	32.5	34.5	36.5	V
Control Function Section (FB Pin)						

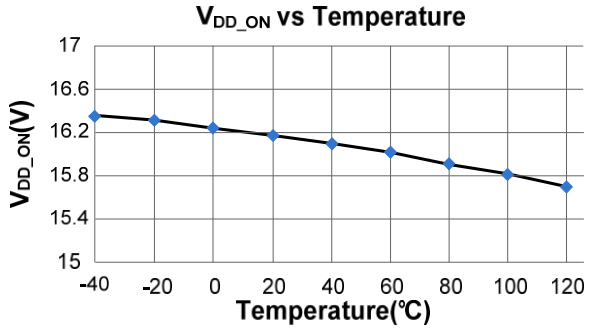
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input		1.98	2.0	2.02	V
V_{FB_SLP}	Short Load Protection (SLP) Threshold			0.85		V
T_{FB_Short}	Short Load Protection (SLP) Debounce Time			35		ms
V_{FB_DEM}	Demagnetization Comparator Threshold			0		mV
T_{off_min}	Minimum OFF time	(Note 3)		2		us
T_{off_max}	Maximum OFF time			2		ms
T_{on_max}	Maximum ON time			36		us
I_{Cable_max}	Maximum Cable Drop compensation current			54		uA
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		0.98	1	1.02	V
T_{D_OCP}	Over Current Detection and Control Delay	GATE=0.5nF		100		ns
Constant Current Section (COMP Pin)						
V_{CC_REF}	Reference for CC Loop		490	500	510	mV
GATE Driver Section (GATE Pin) (Note 3)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650			V
R_{DSON}	Static Drain-Source On Resistance			0.9	0.95	Ohm
Over Temperature Protection						
T_{SD}	Thermal Shutdown	(Note 3)	---	165	--	°C
T_{RC}	Thermal Recovery	(Note 3)		135	--	°C

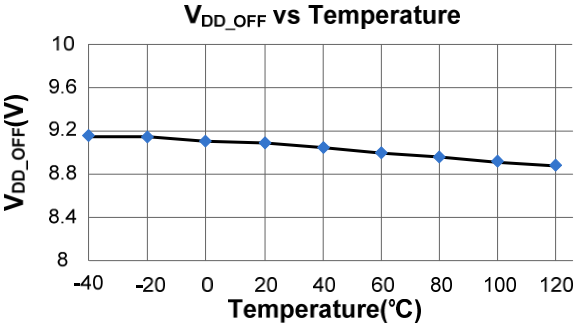
Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

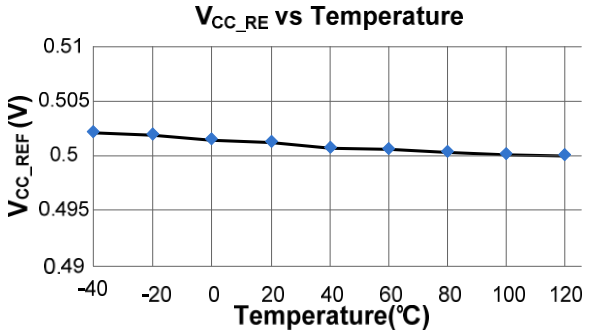
Note2. The device is not guaranteed to function outside its operating conditions.

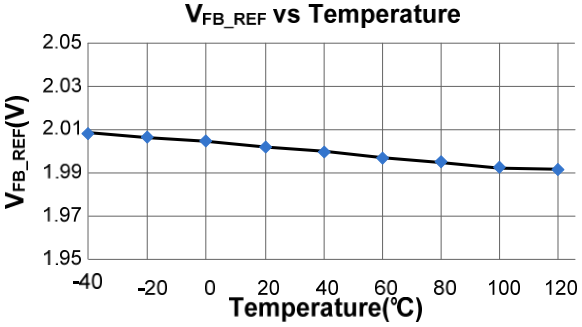
Note3. Guaranteed by the Design.

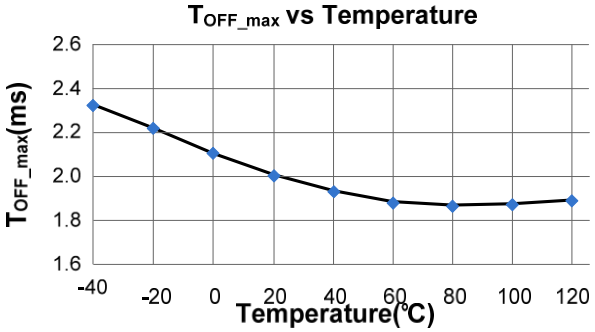
Characterization Plots

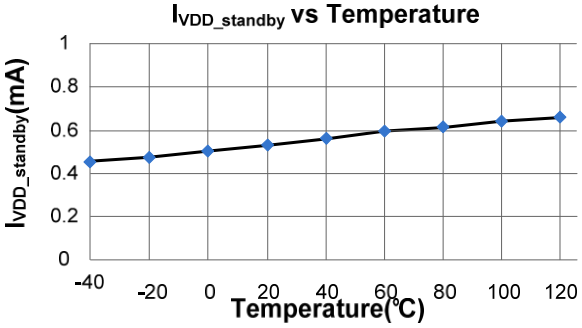












Operation Description

DP5546 a high performance, multi mode, highly integrated Quasi Resonant Primary Side Regulation (QR-PSR) controller. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

System Start-Up Operation

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches UVLO turn-on voltage of 16.3V (typical), DP5546 begins switching and the IC operation current is increased to be 1mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

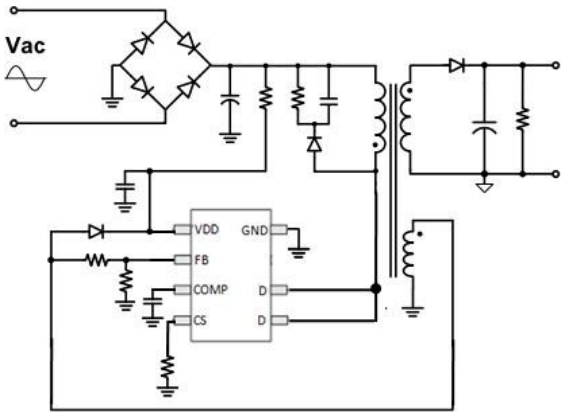


Fig.1

Once DP5546 enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 0.5mA typically, which helps to reduce the standby power loss.

PSR Constant Voltage Modulation (PSR-CVM)

In primary side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates the CV sampling signal timing waveform in DP5546. As shown in Fig.2,it is clear that there is a down slope representing a decreasing total rectifier Vf and its voltage drop as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the CV sampling signal blocks the leakage inductance reset and ringing. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the Primary Side Constant Voltage Modulator (PS-CVM) for CV control. The internal reference voltage for EA is trimmed to 2V with high accuracy.

During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for “demagnetization plateau”, where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively.

When system enters over load condition, the output voltage falls down and the FB sampled voltage should be lower than 2V internal reference which makes system enter CC Mode automatically.

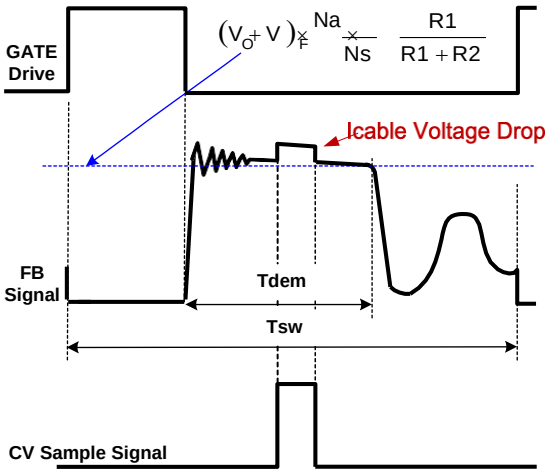


Fig.2

Constant Current Regulation

DP5546 can accurately control the output current by the internal current feedback control loop. The output mean current in constant current (CC) mode can be approximately expressed as:

$$I_{CC\_OUT}(mA) \cong \frac{N}{2} \times \frac{500mV}{Rcs(\Omega)}$$

In the equation above,

N---The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power MOSFET source to GND.

Multi Mode Control in CV Mode

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in DP5546 which is shown in the Fig 3.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.

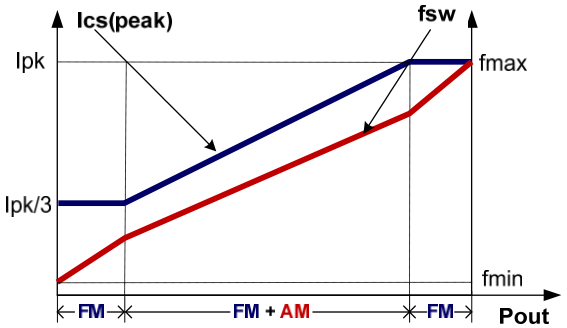


Fig.3

Programmable Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In DP5546, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.4) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in Fig.4), the cable loss compensation can be programmed. The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

For example, R1=3 KΩ, R2=18KΩ, The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} = \frac{54uA \times (3K//18K)}{2V} \times 100\% = 6.9\%$$

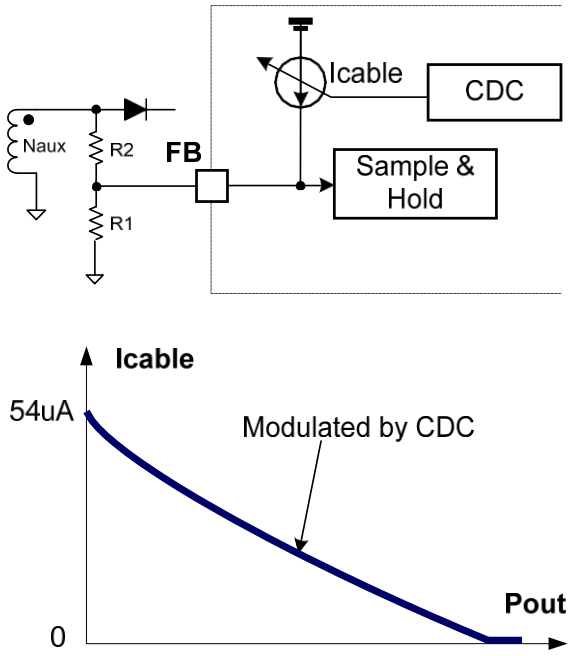


Fig.4

- **Optimized Dynamic Response**

In DP5546, the dynamic response performance is optimized to meet USB charge requirements.

- **Audio Noise Free Operation for PSR**

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation. In DP5546, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **Short Load Protection (SLP)**

In DP5546, the output is sampled on FB pin and then compared with a threshold of UVP (1.05V typically) after an internal blanking time (35ms typical).

In DP5546, when sensed FB voltage is below 0.85V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 30V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 9V) and then the system will restart up again. An internal 34.5V (typical) zener clamp is integrated to prevent the IC from damage.

- **On Chip Thermal Shutdown (OTP)**

When the IC temperature is over 165 ^{o}C, the IC shuts down. Only when the IC temperature drops to 135 ^{o}C, IC will restart.

- **Pin Floating Protection**

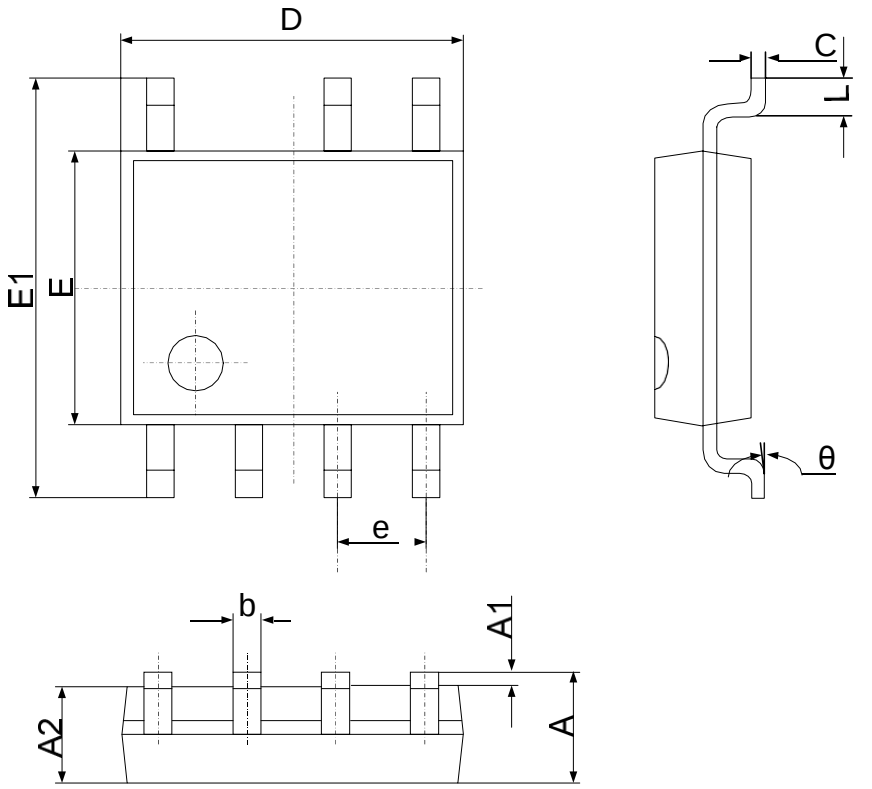
In DP5546, if pin floating situation occurs, the IC is designed to have no damage to system.

- **Soft Totem-Pole Gate Driver**

DP5546 has a soft totem-pole gate driver with optimized EMI performance.

Package Dimension

DIP7



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

Revision History

DATE	REV.	DESCRIPTION	Framer	Approver
2019/09/26	1.0	First Release	Zhou Hui	Xu Yan